Addressing and Data Modes in Muon VME Crates

Up to date there are several VME modules constituting Muon Readout Crates and Muon Front-End Crates. All muon VME electronics uses 9U x 280mm Euroboard mechanical hardware with standard J1/J2 VME connectors. Some of the Muon Readout Crate modules are legacy of Run I, others are new modules designed for upgrade. In order to provide full compatibility with old and new designs the following rules have to be observed when designing VME modules for Muon VME Crates.

- All status and control registers have to be accessible via standard A24:D16 data mode
- Short I/O data addressing mode must be avoided, unless it is specifically required by D0 specifications
- Byte wide data access mode D08(OE) is not necessary to implement as required my the VME standard, unless it is specifically required by D0 specifications

Muon Front-End Crates employ custom J3 backplanes, but otherwise are electrically compatible with VME standard IEEE 1014-1987 with a few minor exceptions. The following is a list of existing or proposed data and addressing modes for <u>Muon Readout Crates only</u>:

- Vertical Interconnect is a A24:D32:D16:D08(EO) master. As a slave it has status registers located in short I/O space and accepts A16:D16:D08(OE) commands. In case when Ethernet interface will be used in VME processors instead of Vertical Interconnect, the latter will not be installed in the Readout Crates.
- 2. VME Buffer Driver is a A24:D32:D16:D08(EO) master. As a master the VBD works in DMA mode using preprogrammed information in word count registers. In run I VBD's DMA controller used word count in short I/O address space and data in standard address space. In Run II we plan to use standard addressing mode to program most of the DMA transfers. Only crate ID data will be retrieved from the MFC's NVRAM in the short I/O addressing mode. VBD's DMA controller supports block and non-block data transfers. As a slave VBD has status registers in short I/O space and accepts A16:D16 commands.
- 3. Muon Fanout Card is a A24:D16 slave. It also has 8 Kbyte non-volatile memory, which is accessible via short I/O space using A16:D16:D08(OE) commands. All MFC's status and control registers are accessible via standard addressing mode with 16-bit data transfers.
- 4. Muon Readout Card is a A24:D32:D16 slave. It has 64K bytes of status registers and memory. MRC's control/status registers can be accessed via 16-bit data transfers and its memory can be accessed via 16- or 32-bit data transfers.
- Readout Crate VME processor (MVME162LX-222a) has a default A32:D32 mode for both master and slave interfaces. Since there is no devices in Muon Readout Crates, which provide A32 mastership, it is changed to a standard A24 mode. A four Mbyte RAM is placed by default at Slave addresses \$00000000- \$003FFFFF. Right now it is re-configured to a

standard \$C00000-\$FFFFFF address range instead. MVME162's Master interface is configurable and will access addresses from \$00000000 to \$00FFFFFF in the standard address mode. Full memory maps for short I/O and standard addressing modes are shown in Table 1 and Table 2 respectively.

Table 1. Muon Readout Crate short I/O address map.

| Address range | Module | Comment |
|---------------|--------|-----------------------|
| \$0000-\$1FFF | N/A | Reserved |
| \$4000-\$41FF | VI | BIM & Interrupt |
| \$8000-\$9FFF | MFC | NVRAM 8 KB |
| \$A000-\$BFFF | VBD | Status registers 8 KB |
| \$C000-\$FFFF | N/A | Reserved |

Table 2. Muon Readout Crate standard address map.

| Address range | Module | Comment |
|-------------------|--------|---------------------------|
| \$000000-\$1FFFFF | N/A | Reserved |
| \$200000-\$20FFFF | TFC | Status registers & memory |
| \$210000-\$21FFFF | MFC | Status registers & FIFOs |
| \$220000-\$2FFFF | MRC | Event buffers & registers |
| \$300000-\$37FFFF | N/A | Reserved |
| \$380000-\$3FFFFF | VBD | Buffer Memory |
| \$000000-\$FFFFF | 162LX | VME Master |
| \$400000-\$BFFFFF | N/A | Reserved |
| \$C00000-\$FFFFF | 162LX | RAM (VME Slave) |

Notes: The current MVME162LX memory range is shown.

Addresses shown are subject to change, if necessary.